2.3.2 Digital Signal Processing

Lecturer	Prof. Dr.-Ing. Dr.h.c. Jürgen Becker
Content	In this course the fundamentals for digital signal processing will be introduced from an computing architecture perspective. The attendance at the lecture affords the comprehension and classification of target architectures as well as partitioning strategies of HW/SW based systems. The accompanying exercises and lab tutorials intend to consolidate the knowledge from the lectures.
Course Objectives	The following selection of topics will be presented: ▪ Fundamentals and classification schemes in computing architectures ▪ Introduction to DSPs, ASIPs, FPGAs and heterogeneous processor architectures ▪ System on Chip design and IP based technologies ▪ Tool- and Design Flows ▪ HW-/SW-Partitioning Technologies.
Learning Targets/ Skills	After course completion, participants should be able to a) perform a basic design space exploration based on their project work, b) do a hardware software partitioning, c) implement basic designs for heterogenous Multi-Core and FPGA based systems, d) communicate effectively with information technologies engineers
Pre-Requisites	Basic knowledge about digital electronics, interest in electronics and technology
Duration	Approx. 3 x 6 h
Teaching Method	Formal lectures, tutorial style discussion, lab work
Course Material	Slides
Literature	
Contact Lecturer	Prof. Dr.-Ing. Dr.h.c. Jürgen Becker, becker@kit.edu

Schedule: Digital Signal Processing	
Institute	**Content (selected keywords)**
Day 1	
	Lecture: Basics on Computing Architectures, Presentation of selected architectures
	Lab: Introduction to FPGA tooling, first excercises
Day 2	
	Lecture: Introduction of selected architectures, SoC design, Heterogeneous multi-core architectures
	Lab: Design for heterogeneous FPGA systems
Day 3	
	Lecture: Fundamentals about toolflows
	Lab: Design for heterogeneous systems